

Attorney's Docket No. 001207.P011

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:)

Peter M. Pani et al.)

Examiner: Not yet assigned

Application No.: 10/814,943)

Art Unit: Not yet assigned

Filed: March 30, 2004)

For: A SCALABLE NON-BLOCKING)
SWITCHING NETWORK FOR)
PROGRAMMABLE LOGIC)

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

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Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the non-patent art. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicants.

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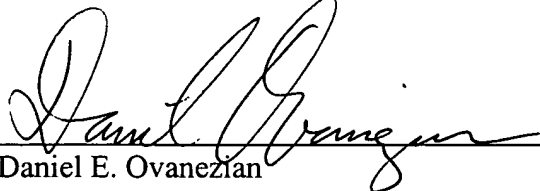
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 4/20, 2004


Daniel E. Ovanezian
Reg. No. 41,236

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 001207.P011	Application Number: 10/814,943
	First Named Inventor: Peter M. Pani	
Filing Date: March 30, 2004		

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		Altera Corporation Date Sheet, Flex EPF81188 12,000 Gate Programmable Logic Device, September 1992, Ver. 1, pp. 1-20.	
		ATMEL Field Programmable Arrays, AT 6000 Series, 1993, p. 1-16.	
		BRITTON, et al., "Optimized Reconfigurable Cell Array Architecture for High-Performance Field Programmable Gate Arrays," Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, 1993, pp. 7.2.1. - 7.2.5.	
		BUFFOLI, E., et al., "Dynamically Reconfigurable Devices Used to Implement a Self-Tuning, High Performances PID Controller," 1989 IEEE, pp., 107-112.	
		BURSKY, D., "Fine-Grain FPGA Architecture Uses Four Levels of Configuration Hierarchy," 2328 Electronic Design, 41, No. 20, Cleveland, OH, October 1, 1993, pp. 33-34.	
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		DEVADES, S., et al., "Boolean Decomposition of Programmable Logic Arrays," IEEE 1988, pp. 2.5.1 - 2.5.5.	
		F. Zlotnick, P. Butler, W. Li, D. Tang, "A High Performance Fine-Grained Approach to SRAM Based FPGAs", p. 321-326, Wescon September 28-30, 1993.	
		LIU, D.L., et al., "Design of Large Embedded CMOS PLA's for Built-In Self-test," IEEE Transactions on Computed-Aided Design, Vol. 7, No. 1, January 1988, pp. 50-53.	
		Minnick, R.C., "A Survey of Microcellular Research", vol. 14, no. 2, 4/1967, pp. 203-241.	

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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

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		Motorola Project Brief, "MPA10xx Field Programmable Gate Arrays," September 27, 1993, 2 pages.	
		Robert H. Krambeck, "ORCA: A High Performance, Easy to Use SRAM Based Architecture", p. 310-320, Wescon September 28-30, 1993.	
		SHOUP, R. G., "Programmable Cellular Logic Arrays," Abstract, Ph.D. Dissertation, Carnegie Mellon University, Pittsburgh, PA, March 1970, (partial) pp. ii-121.	
		Sinan Kaptanoglu, Greg Bakker, Arun Kundu, Ivan Corneillet, Ben Ting, "A New High Density and Very Low Cost Reprogrammable FPGA Architecture", 10 pages, Actel Corporation.	
		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits," Contract No. AF 19 (628) 2907, Project No. 4645, Task No. 464504, Final Report, November 30, 1965.	
		SUN, Y., et al., "An Area Minimizer for Floorplans with L-Shaped Regions," 1992 International Conference on Computer Design, 1992 IEEE, pp. 383-386.	
		VIDAL, J. J., "Implementing Neural Nets with Programmable Logic," IEEE Transactions on Acoustic, Speech, and Signal Processing, Vol. 36, No. 7, July 1988, pp. 1180-1190.	
		Wang, P. et al. IEEE, "A High Performance FPGA with Hierarchical Interconnection Structure", pp. 239-242 (May 30, 1994).	
		Xilinx, "The Programmable Gate Array Data Book", 1992.	

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